In the Claims:

Please cancel Claims 1 and 2.

3. (currently amended) ~~The method of claim 1, further comprising:~~ A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

providing ~~spacers~~ spacers along sidewalls of the patterned conductive ~~layer,~~ layer;

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch; and

performing a second etch of the high-k dielectric layer to remove at least part of the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch, wherein the first and second etches of the high-k dielectric layer are performed, at least in part, in alignment with the spacers.

4. (currently amended) The method of ~~claim 1,~~ claim 3, wherein the first etch is a dry etch process.

5. (original) The method of claim 4, wherein the dry etch process is a reactive ion etching process using an etch chemistry comprising at least one of inert gas, chlorine, and fluorine.

6. (currently amended) The method of ~~claim 1,~~ claim 3, wherein the second etch is a wet etch process.

7. (original) The method of claim 6, wherein the wet etch process uses an etch chemistry comprising an inorganic acid.

8 (original) The method of claim 7, wherein the inorganic acid comprises at least one of a halogen acid, HF, and H_2SO_4.

9. (currently amended) ~~The method of claim 1,~~ A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch; and

performing a second etch of the high-k dielectric layer to remove at least part of the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch, wherein the patterning of the conductive layer, the first etch, and the second etch are performed in a same chamber.

10. (currently amended) ~~The method of claim 1, further comprising:~~ A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch;

performing a second etch of the high-k dielectric layer to remove at least part of the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch; and

plasma ashing the remaining portion of the high-k dielectric layer after the first etch and before the second etch.

11. (currently amended) The method of ~~claim 1~~ claim 3, wherein the high-k dielectric material comprises at least one of an aluminum oxide, a zirconium oxide, a hafnium oxide, a hafnium silicate, a zirconium silicate, a silicon nitride, a tantalum oxide, a barium strontium titanate, and a lead-lanthanum-zirconium-titanate.

12. (currently amended) ~~The method of claim 1, further comprising:~~ A method of fabricating a semiconductor device, comprising:

providing a layer of high-k dielectric material over a substrate;

providing a layer of conductive material over the high-k dielectric layer;

patterning the conductive layer;

performing a first etch on the high-k dielectric layer, wherein a portion of the high-k dielectric layer being etched with the first etch remains after the first etch;

changing material properties of the remaining portion of the high-k dielectric layer during the first ~~etch.~~ etch; and

performing a second etch of the high-k dielectric layer to remove at least part of the remaining portion of the high-k dielectric layer, wherein the second etch differs from the first etch.

13. (currently amended) The method of ~~claim 1~~ claim 3, wherein the high-k dielectric layer is provided using a process selected from a group consisting of chemical vapor deposition, metal-organic chemical vapor deposition, atomic layer deposition, atomic layer chemical vapor deposition, low pressure chemical vapor deposition, sputtering, and anodization.

14. (currently amended) The method of ~~claim 1~~ claim 3, wherein the high-k dielectric layer has an initial thickness prior to the first etch, wherein the remaining portion of the high-k dielectric layer has a first thickness after the first etch, the first thickness being about half the initial thickness.

Please cancel Claims 15-22.

23. (new) The method of claim 9, wherein the first and second etches of the high-k dielectric layer are performed in alignment with the patterned conductive layer.

24. (new) The method of claim 9, wherein the first etch is a dry etch process.

25. (new) The method of claim 9, wherein the second etch is a wet etch process.

26. (new) The method of claim 9, further comprising:

plasma ashing the remaining portion of the high-k dielectric layer after the first etch and before the second etch.

27. (new) The method of claim 9, further comprising:

changing material properties of the remaining portion of the high-k dielectric layer during the first etch.

28. (new) The method of claim 10, wherein the first and second etches of the high-k dielectric layer are performed in alignment with the patterned conductive layer.

29. (new) The method of claim 10, wherein the first etch is a dry etch process.

30. (new) The method of claim 10, wherein the second etch is a wet etch process.

31. (new) The method of claim 10, wherein the patterning of the conductive layer, the first etch, and the second etch are performed in a same chamber.

32. The method of claim 10, further comprising:

changing material properties of the remaining portion of the high-k dielectric layer during the first etch.

33. (new) The method of claim 12, wherein the first and second etches of the high-k dielectric layer are performed in alignment with the patterned conductive layer.

34. (new) The method of claim 12, wherein the first etch is a dry etch process.

35. (new) The method of claim 12, wherein the second etch is a wet etch process.

36. (new) The method of claim 12, wherein the patterning of the conductive layer, the first etch, and the second etch are performed in a same chamber.

37. (new) The method of claim 12, further comprising:

plasma ashing the remaining portion of the high-k dielectric layer after the first etch and before the second etch.